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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/735,374	12/12/2003	Betty Shu Mercer	TI-36853	1822

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TEXAS INSTRUMENTS INCORPORATED
P O BOX 655474, M/S 3999
DALLAS, TX 75265

EXAMINER	
ANDUJAR, LEONARDO	

ART UNIT	PAPER NUMBER
2826	

NOTIFICATION DATE	DELIVERY MODE
04/17/2009	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

uspto@ti.com

Office Action Summary	Application No.	Applicant(s)	
	10/735,374	MERCER ET AL.	
	Examiner	Art Unit	
	Leonardo Andújar	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 January 2009*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,7,16,17,19-21,23,33-35 and 38* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,7,16,17,19-21,23,33-35 and 38* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

1. Applicant's election without traverse of claims 1-3, 7, 16, 17 and 19-23 in the reply filed on 06/27/2006 is acknowledged.

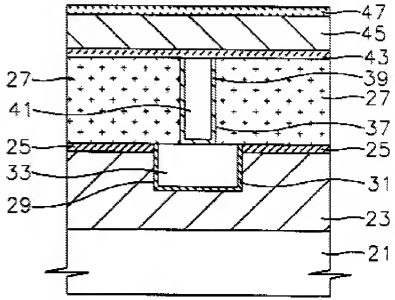
Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1, 7, 33, 34 and 38 rejected under 35 U.S.C. 103(a) as being unpatentable over Jeong (US 6,545,358) in view of Sung et al. (US 6,171,927).

4. Regarding claim 1, Jeong (e.g. fig. 2) shows an integrated circuit, comprising: a semiconductor substrate 21 comprising device elements and one or more metallization layers interconnecting the device elements and having an uppermost layer 23 comprising bond pads 33 (e.g. tungsten); a protective overcoat 27 formed over the metallization layers, the protective overcoat having vias 37 through it; a conductive barrier layer 39 conformal to the via, a bottom surface of the conductive barrier abutting at least one of the bond pad; tungsten plugs 41 substantially filling the vias; and thick copper 45 formed over the protective overcoat and forming connections to the tungsten plugs (clms. 1, 4 and18).



Jeong does not explicitly disclose material selection for overcoat 27 (inter layer insulating). Shih teaches that silicon oxynitride and silicon nitride are suitable materials for making interlayer insulating (see claim 3). It would have been obvious to one having ordinary skill in the art at the time the invention was made to make the protective overcoat of Jeong of silicon oxynitride or silicon nitride due to their relative high dielectric constant and cost. Also, it has been held to be within the general skill of a worker in the art to select a known material on the basis of its suitability for the intended use as a matter of obvious design choice. *In re Leshin, 125 USPQ 416.* Moreover, the claim would have been obvious to because a particular known technique was recognized as part of the ordinary capabilities of one skilled in the art see *KSR International Co. v. Teleflex Inc., 550 U.S.-, 82 USPQ2d 1385(2007).* In this case, silicon oxynitride and silicon nitride are standard materials for interlayer dielectric layers.

5. Regarding claims 7, Jeong teaches that the thick copper forms interconnections between device elements within the integrated circuit (col. 1/lls. 55-62).

6. Regarding claim 33, Jeong in view of Thomas in view of Sung further in view of Shih show that the tungsten plug is electrically couple at leas one of the thick copper connections to one of the metal regions.

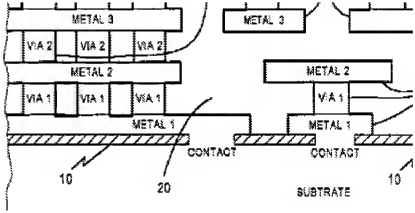
7. Regarding claim 34, Jeong in view of Thomas further in view of Sung further in view of Shih shows that the thick copper substantially overlies at least one of the metal regions.

8. Regarding claim 38, Jeong teaches a copper seed layer 43 formed directly onto the surface of each of the tungsten plugs, wherein the copper seed layer comprises a conductive barrier (e.g. TiN) layer to prevent copper from diffusing into the protective overcoat (col. 3/lls. 66-67 & col. 4/ll. 1).

9. Claims 16, 19-21 and 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jeong (US 6,545,358) in view of Buynoski (US 6,218,282) further in view of Shih (US 5,827,782).

10. Regarding claims 16 and 20, Jeong (e.g. fig. 3) shows an integrated circuit, comprising: a semiconductor substrate 21 comprising device elements and one or more metallization layers interconnecting the device elements and having an uppermost layer 23-51 comprising pads; a protective overcoat 27 formed over the metallization layers, the protective overcoat having vias 37 through it; wherein the array of vias are formed over individual bond pads, tungsten plugs 41 substantially filling the vias and connecting to the uppermost layer bond pads; and thick copper 45 formed over the protective

overcoat and forming connections to the tungsten plugs (clm. 1 and 18). Jeong does not teach that multiple vias are formed over individual bond pad or the material for making the protective overcoat 27. Nonetheless, Buynoski (e.g. fig. 4) shows an integrated circuit having multiple vias 1 formed over individual bond pads (metal 1).



Shih teaches that silicon oxynitride and silicon nitride are suitable materials for making interlayer insulating (see claim 3).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to form multiple vias over individual bond pads disclosed by Jeong a suggested by Buynoski to increase device density and performance, and to make the protective overcoat of Jeong in view of Buynoski of silicon oxynitride or silicon nitride due to their relative high dielectric constant and cost. Also, it has been held to be within the general skill of a worker in the art to select a known material on the basis of its suitability for the intended use as a matter of obvious design choice. *In re Leshin, 125 USPQ 416.* Moreover, the claim would have been obvious to because a particular known technique was recognized as part of the ordinary capabilities of one skilled in the art see *KSR International Co. v. Teleflex Inc., 550 U.S.-, 82 USPQ2d 1385(2007).* In

this case, silicon oxynitride or silicon nitride are standard materials for interlayer dielectric layers.

11. Regarding claim 19, Jeong teaches that the plug is made of tungsten with have a coefficient of thermal expansion less than or equal to about 8 ppm/C.

12. Regarding claim 21, Jeong teaches that the uppermost layer is an aluminum metallization (col.3/lls. 9-10).

13. Regarding claim 23, Jeong teaches that the thick copper forms interconnections between device elements within the integrated circuit (col. 1/lls. 55-62).

14. Claim 17 is rejected under 35 U.S.C. 103(a) as being unpatentable over Jeong (US 6,545,358) in view of Buynoski (US 6,218,282) further in view of Shih (US 5,827,782) further in view of Ting et la. (US 5,969,422).

15. Regarding claim 17, Jeong in view of Buyoski further in view Shih discloses the claimed invention except for a plug made of copper. Ting teaches that copper is a suitable material for contact plugs (abstract, col. 6/lls. 10-15)). It would have been obvious to one having ordinary skill in the art at the time the invention was made to make the contact plug disclosed by Jeon in view of Buynoski of copper as suggested by Ting, since it has been held to be within the general skill of a worker in the art to select a known material on the basis of its suitability for the intended use as a matter of obvious design choice. *In re Leshin, 125 USPQ 416.*

16. Claim 35 is rejected under 35 U.S.C. 103(a) as being unpatentable over Jeong (US 6,545,358) in view of Thomas et al. (US 5,117,276) further in view of further in view

of Sung et al. (US 6,171,927) further in view of Sung et al. (US 6,171,927) further in view of Shin (US 5,827,782) further in view of Or-Bach et al. (US 6,476,493).

17. Regarding claim 35, Jeong in view of Thomas further in view of Sung further in view of Shih teaches most aspects of the instant invention including a thick copper but does not explicitly teaches that the thick copper layer does not extend over at least a portion of the dielectric region. However, it is implicitly disclosed because metal interconnections are arranged as grid type array. Therefore, it is not possible for a layer to overlay the whole surface of the integrated circuit unless the layer is a metal plane. For example Or-Barch (e.g. fig. 3) shows the different interconnection metal levels interconnected by vias wherein an upper layer does not extend over the dielectric regions of a lower level (i.e. the space defined by at least two metal layers in the same level). It would have been obvious to one having ordinary skill in the art at the time the invention was made to make the thick copper layer such as to do not extend over at least a portion of the dielectric region disclosed by Jeong in view of Thomas further in Sung further in view of Shih to provide an interconnection system which has minimal parasitic capacitance and it is mechanically strong.

Response to Arguments

18. Applicant's arguments with respect to claim 16 have been considered but are moot in view of the new ground(s) of rejection.

19. Applicant argues that the claim interpretation urged in the pending OA (in which the metal 1 region is deemed a bond pad) is inconsistent with the plain meaning of the term 'bond pad' as understood by a person of ordinary skill in the art. However, this is

not found persuasive since the layer 1 of Buynoski complies with the ordinary meaning of bond pad (see definition in page 12 of applicant remarks received on 1/22/2009). According to applicant the layer 1 disclosed by Buynoski does not agree with applicant provided definition of bond pad: "relatively large metal areas on a die used for electrical contact with a package or probe pins" (accessed at http://www.sematech.orq/publications/dictionary/b.htm on Jan. 16, 2008). However, this definition neither apply to "bond pad" of the present invention because the "bond pad 13" disclosed by applicant's specification is not nor can be used for electrical contact with a package or probe pins. Note that the interconnection structure formed over the pad make impossible to form a direct electrical contact with a package or probe pins. The "bonding pad" disclosed by applicant is a metal layer large enough for having plural metal plugs formed on its surface (see fig. 4, layer 13). The disclosed bond pad is structurally identical to the layer 1 disclosed by Buynoski's figure 4 where plural vias1 have been formed on its surface. Although Applicant argues that there is a considerable size difference between the claimed bond pad and layer 1, the claim does not recite any dimension or any structural limitation precluding the legitimate interpretation given to the term in the present OA. Applicant argues that specification discloses that the area of the pad is about 60-100 µm square. However, this limitation is not recited. Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

Conclusion

20. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

21. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Leonardo Andújar whose telephone number is 571-272-1912. The examiner can normally be reached on Mon through Thu from 9:00 AM to 7:30 PM EST.

22. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sue Purvis can be reached on 571-272-1236. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

23. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for

published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Leonardo Andújar/
Primary Examiner, Art Unit 2826